Claims

1. A method for plating copper conductors on an electronic substrate comprising the steps of:

providing an electroplating Cu bath filled with an electroplating solution,

maintaining said electroplating solution at a temperature between about 0°C and about 18°C, and

electroplating a Cu layer on said electronic substrate immersed in said electroplating solution.

2. A damascene or dual damascene interconnect structure fabricated by the method of claim 1.

3. A method for plating Cu conductors on an electronic substrate according to claim 1 further comprising the step of maintaining said electroplating solution at a temperature preferable between about 5°C and about 15°C.

4. A method for plating Cu conductors on an electronic substrate according to claim 1 further comprising the step of maintaining said electroplating solution at a temperature more preferably between about 8°C and about 12°C.

5. A method for plating Cu conductors on an electronic substrate comprising the steps of:

providing a Cu electroplating solution in a plating bath,

adding an additive to said Cu electroplating solution to a concentration of not more than 5 mL/L,

maintaining said Cu electroplating solution at a temperature not higher than 18°C, and

electroplating a Cu layer on said electronic substrate immersed in said Cu electroplating solution.

6. A method for plating Cu conductors on an electronic substrate according to claim 1 further comprising the step of maintaining an additive concentration in said electroplating solution at not more than 15 mL/L.

7. A method for plating Cu conductors on an electronic substrate according to claim 5, wherein said additive is added to said electroplating solution to a concentration of not more than 3 mL/L MLo.

8. A method for plating Cu conductors on an electronic substrate according to claim 5, wherein said additive is added to said electroplating solution to a concentration of not more than 15 mL/L MD.

9. A method for plating Cu conductors on an electronic substrate according to claim 1 further comprising the step of maintaining a wafer rotational speed at less than 100 RPM.

10. A method for plating Cu conductors on an electronic substrate according to claim 1 further comprising the step of maintaining a plating current density of at least 15 mA/cm^2.

11. A method for plating Cu conductors on an electronic substrate according to claim 1 further comprising the step of maintaining a deposition rate of at least 5 nm/sec.

12. A method for plating Cu conductors on an electronic substrate according to claim 1 further comprising the step of electroplating a Cu layer to a thickness of at least 0.5 μm.

13. A method for plating Cu conductors on an electronic substrate according to claim 1 further comprising the steps of:

maintaining a additive concentration in said electroplating solution at not more than 15 mL/L,

maintaining a wafer rotational speed at less than 100 RPM,

maintaining a plating current density of at least 15 mA/cm^2, and

maintaining a deposition rate of at least 5 nm/sec.

14. A method for plating Cu conductors on an electronic substrate according to claim 5 further comprising the step of maintaining a wafer rotational speed at less than 100 RPM.

15. A method for plating Cu conductors on an electronic substrate according to claim 5 further comprising the step of maintaining a plating current density of at least 15 mA/cm^2.

16. A method for plating Cu conductors on an electronic substrate according to claim 5 further comprising the step of maintaining a deposition rate of at least 5 nm/sec.

17. A method for plating Cu conductors on an electronic substrate according to claim 5 further comprising the step of electroplating a Cu layer to a thickness of at least 0.5 μm.

18. A method for plating Cu conductors on an electronic substrate according to claim 5 further comprising the steps of:

maintaining a wafer rotational speed at less than 100 RPM,

maintaining a plating current density of at least 15 mA/cm^2,

maintaining a deposition rate of at least 5 nm/sec, and

electroplating a Cu layer to a thickness of at least 0.5 μm.

19. A method for plating Cu conductors on an electronic substrate comprising the steps of:

depositing a first layer of Cu on said electronic substrate in a first electroplating solution containing a first additive concentration, and

depositing a second layer of Cu on top of said first layer of Cu in a second electroplating solution containing a second additive concentration smaller than said first dopant concentration.

20. A method for plating Cu conductors on an electronic substrate according to claim 19 further comprising the step of plating a dual damascene structure of trench/via.

21. A method for plating Cu conductors on an electronic substrate according to claim 19 further comprising the step of depositing said first layer of Cu in a via hole having an aspect ratio of diameter/depth of at least 1/3.

22. A method for plating Cu conductors on an electronic substrate according to claim 19 further comprising the step of depositing said second layer of Cu in a second electroplating solution maintained at a temperature of not higher than 18°C.

23. A method for plating Cu conductors on an electronic substrate according to claim 19 further comprising the step of depositing said second layer of Cu in a second electroplating solution with said substrate rotating at a rotational speed of less than 100 RPM.

24. A method for plating Cu conductors on an electronic substrate according to claim 19 further comprising the step of depositing said second layer of Cu in a second electroplating solution maintained at a plating current density of a least 15 mA/cm^2.

25. A method for plating Cu conductors on an electronic substrate according to claim 19 further comprising the step of depositing said second layer of Cu in a second electroplating solution at a deposition rate of at least 5 nm/sec.

26. A method for plating Cu conductors on an electronic substrate according to claim 19 further comprising the step of depositing said second layer of Cu in a second electroplating solution to a thickness of at least 0.5 μm.

27. A method for plating Cu conductors on an electronic substrate according to claim 19 further comprising the steps of depositing a second Cu layer on top of said first Cu layer in a second electroplating solution containing a second additive concentration smaller than said first dopant concentration,

maintaining said solution at a temperature not higher than 18°C,

rotating said substrate at a speed of less than 100 RPM,

conducting said plating at a current density of at least 15 mA/cm^2,

depositing said Cu layer at a deposition rate of at least 5 nm/sec.

28. A semiconductor structure of a damascene or dual damascene interconnect formed by a trench-filling process of electroplated Cu having an as-deposited grain size of not less than 0.5 μm and a decrease in electrical resistance of at least 15% after a time period of not more than 30 hours at about 21°C.

29. A semiconductor structure of a damascene or dual damascene interconnect according to claim 28, wherein said as-deposited grain size of electroplated Cu is between about 0.5 μm and about .15 μm.

30. A semiconductor structure of a damascene or dual damascene interconnect according to claim 28, wherein said grain size of said electroplated Cu after said time period of not more than 30 hours at about 21°C is between about 1.5 μm and about 2 μm.